Docket No.: LGS/S-0030A PATENT

#14/C
3/26/3
Jules

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Joo-Hyong LEE	:	
Serial No. 09/955,288	:	Group Art Unit: 2815
Confirm. No.: 9373	:	Examiner: Jose R. Diaz
Filed: September 19, 2001	:	
For: LATCH-UP RESISTANT CMOS STRUCTURE	:	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

Prior to initial examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 1-5, and 11-25 as follows:

Sub D7

C1

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a first conductivity type;

a first well having a second conductivity type formed in a first region in a major surface of the semiconductor substrate;

a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well; and